7 SEGMENT NUMERIC, UP TO 8-DIGIT DISPLAY DRIVER
10MHz I/O, LOW EMI & LOW SLEW-RATE LIMITED

A8478

Description

The A8478 is compact display driver for 7-segment numeric displays of up to 8 digits. The A8478 can be programmed via SPI, QSPI, and Microwire as well as a conventional 4-wire serial interface.

The A8478 includes an integrated BCD code-B/HEX decoder, multiples scan circuitry, segment and display drivers, and a 64-bit memory. Internal memory stores the LED settings, eliminating the need for continuous device reprogramming.

Every segment can be individually addressed and updated separately. Only one external resistor (R_{SET}) is required to set the current through the LED display. LED brightness can be controlled by analog or digital means. The device can be programmed to use the internal code-B/HEX decoder to display numeric digits or to directly address each segment.

The A8478 features an extremely low shutdown current of typically 3uA, and an operational current of less than 500uA. The number of digits can be programmed, the device can be reset by software, and an external clock is also supported. Additionally, segment blinking can be synchronized across multiple drivers.

The A8478 provides several test modes for easy application debugging.

The A8478 is available in 24-pin Narrow DIP and 24-pin SOP package.

Ordering Information

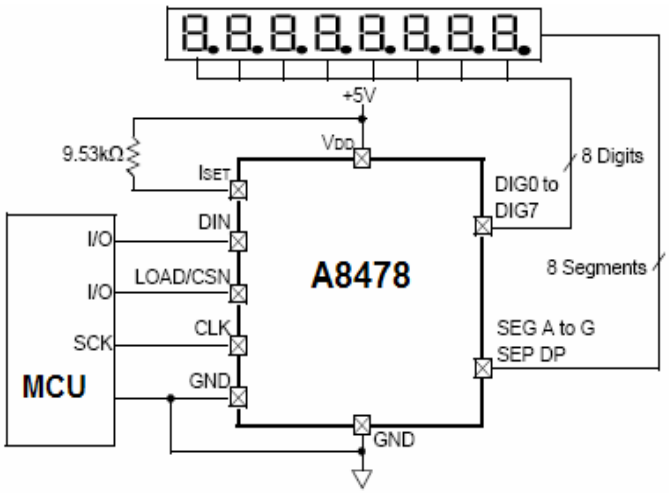
24pin Narrow DIP	A8478PN24-A/B(Tube)
24pin SOP	A8478M24-A /B (Tube) A8478MR24-A/B(T/R)

Features

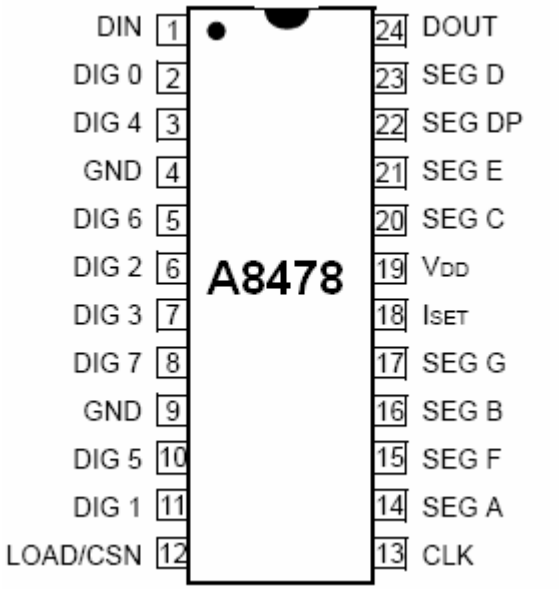
- 10MH$_Z$ SPI-, QSPI-, Microwire-Compatible Serial I/O
- Individual LED Segment Control
- Segment Blinking Control (can be synchronized across multiple drivers)
- Hexadecimal-or BCD-Code/No-Decode Digit Selection
- 3 uA Low-Power Shutdown Current (typ; data retained)
- Extremely Low Operating Current 0.5mA in Open-Loop
- Digital and Analog Brightness Control
- Display Blanked on Power-Up
- Drive Common-Cathode LED Displays
- Low-EMI Low Slew-Rate Limited Segment Drivers(A8478-A)
- Supply Voltage Range: +2.7 to +5.5V
- Software Reset
- Optional External Clock
- 24pin Narrow DIP and SOP Packages

Application

- Bar-Graph Displays
- Instrument-Panel Meters
- LED Matrix Displays
- Dot Matrix Displays
- STB, Audio Equipment



Pin Description



Pin #	Name	Function
1	D_{IN}	Serial-Data Input. Data is loaded into the internal 16-bit shift register on the rising edge of pin CLK
2,3,5,6,7, 8,10,11	DIG 0 :DIG 7	Digit Drive Lines. 8 Eight-digit drive lines that sink current from the display common cathode. The A8478-B pulls the digit outputs to V_{DD} when turned off. The A8478-A digit drivers are high-impedance when turned off.
4,9	GND	Ground. Both GND pins must be connected
12	LOAD/CSN	Load-data input (A8478-B only). The last 16 bits of serial data are latched on the rising edge of this pin.
		Chip-Select Input (SPI-enabled only). Serial data is loaded into the shift register while this pin is low. The last 16 bits of serial data are latched on the rising edge of this pin.
13	CLK	Serial-Clock Input. $10MH_Z$ maximum rate. Data is shifted into the internal shift register on the rising edge of this pin. Data is clocked out of pin D_{OUT} on the falling edge of this pin. On the device SPI-enabled, the CLK input is active only while LOAD/CSN is low.
14,15,16, 17,20,21, 22,23,	SEG A:SEG G SEG DP	7 Segment and Decimal Point Drive Lines. 8 seven-segment drives and decimal point drive that source current to the display. On the A8478-B, when a segment driver is turned off it is pulled to GND. The A8478-A segment drivers is high-impedance when turned off.
18	I_{SET}	Set Segment Current. Connect to V_{DD} through R_{SET} to set the peak segment current (see Selecting Resistor Value and Using External Drivers)
19	V_{DD}	Positive Supply Voltage. Connect to +2.7V to +5.5V supply.
24	D_{OUT}	Serial-Data Output. The data into pin D_{IN} is valid at pin D_{OUT} 16.5 clock cycles later. This pin is used to daisy-chain several the A8478 and is never high-impedance.

Absolute Maximum Ratings

Parameter		Min	Max	Unit	Notes
Voltage (with respect to GND)	V_{DD}	-0.3	7	V	
	DIN,CLK,LOAD/ CSN	-0.3	7	V	
	All other Pins	-0.3	7or V_{DD}+0.3	V	
Current	DIG 0:DIG7 Sink Current		500	mA	
	SEG A:SEG G, SEG DP		100	mA	
Continuous Power Dissipation (T_{AMB}=+85°C)	24Pin Narrow DIP		1066	mW	Derate 13.3mW/℃ above +70℃
	24Pin SOP		941	mW	Derate 11.8mW/℃ above +70℃
Operating Temperature Ranges (T_{MIN} to T_{MAX})	A8478-B	-40	+85	℃	
	A8478-A	0	+70	℃	
Storage Temperature Range		-65	+150	℃	
Package Body Temperature (24Pin SOP)			+260	℃	
Soldering Temperature (24Pin Narrow DIP)			+260	℃	
Humidity		5	85	%	Non-condensing
Electrostatic Discharge	Digital Outputs		1000	V	
	All Other Pins		1000	V	
Latch-Up Immunity			±200	mA	All pins. Except A8478-B pin 11: ±180mA

Note: Stresses beyond may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

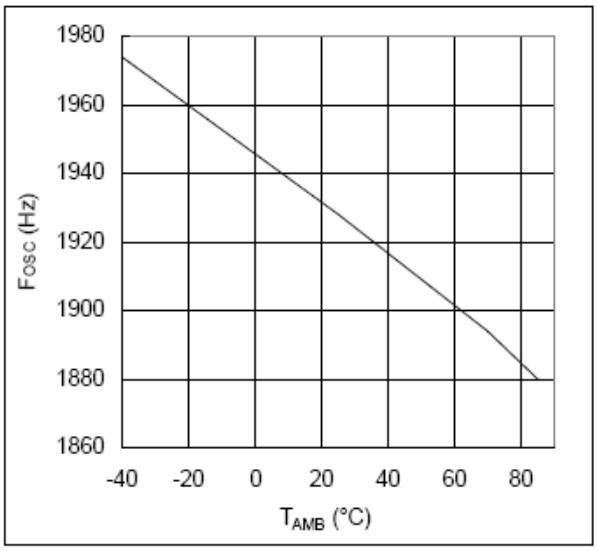
(V_{DD}=2.7 to 5.5V, R_{SET}=9.53kΩ±1%, T_{AMB}=T_{MIN} to T_{MAX})

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Supply Current	I_{DD}	R_{SET}=open circuit			1	mA
		All Segments and decimal point on; I_{SEG}=-40mA		330		
Display Scan Rate	f_{OSC}	8 digits scanned	1000	800	1300	Hz
Digit Drive Sink Current	I_{DIGIT}	V_{OUT}=0.65V	320			mA
Segment Drive Source Current	I_{SEG}	V_{DD}=5.0V, Vout=(V_{DD}-1V)	-30	-40	-45	mA
Segment Current Slew Rate (A8478-A only)	$\triangle I_{SEG}/\triangle t$	T_{AMB} = +25℃, V_{DD} =5.0V, V_{OUT} = (V_{DD}-1V)	10	20	50	mA/us
Segment Drive Current Matching	$\triangle I_{SEG}$			3.0		%
Digit Drive Leakage (A8478-A only)	I_{DIGIT}	Digit off, V_{DIGIT}=V_{DD}			-10	uA
Segment Drive Leakage (A8478-A only)	I_{SEG}	Segment off, V_{SEG}=0V			1	uA
Digit Drive Source Current (A8478-A only)	I_{DIGIT}	Digit off, V_{DIGIT}=(V_{DD}-0.3V)	-2			mA
Segment Drive Sink Current (A8478-A only)	I_{SEG}	Segment off, V_{SEG}=0.3V	5			mA
Slow Segment Blink Period (ON phase, Internal Oscillator)	$t_{SLOWBLINK}$		0.64	1	1.65	S
Fast Segment Blink Period (ON phase, Internal Oscillator)	$t_{FASTBLINK}$		0.32	0.5	0.83	S
Fast or Slow Segment Blink Duty Cycle (Guaranteed by design)			49.9	50	50.1	%
Logic Inputs/Outputs						
Input Current DIN,CLK,LOAD/CSN	I_{IH}, I_{IL}	V_{IN}=0V or V_{DD}	-1		1	uA
Logic High Input Voltage	V_{IH}		0.7x V_{DD}			V
Logic Low Input Voltage	V_{IL}	V_{DD}=5.0V±10%			0.8	V
		V_{DD}=3.0V±10%			0.6	
Output High Voltage	V_{OH}	D_{OUT}, I_{SOURCE}=-1mA V_{DD}=5.0V±10%	V_{DD}-1			V
		D_{OUT}, I_{SOURCE}=-1mA V_{DD}=3.0V±10%	V_{DD} -0.5			
Output Low Voltage	V_{OL}	D_{OUT}, I_{SINK}=1.6mA			0.4	V
Hysteresis Voltage	$\triangle V_I$	D_{IN}, CLK, LOAD/CSN		1		V
Timing						
CLK Clock Period	t_{CP}		100			ns
CLK Pulse Width High	t_{CH}		50			ns
CLK Pulse Width Low	t_{CL}		50			ns
CSM Fall-to-CLK Rise Setup Time(A8478 SPI-programmed)	t_{CSS}		25			ns
CLK Rise to LOAD/CSN Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		25			ns
DIN Hold Time	t_{DH}		0			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD}=50pF			25	ns
LOAD Rising Edge to Next Clock Rising Edge(A8478-B only)	t_{LDCK}		50			ns
Minimum LOAD/CSN Pulse High	t_{CSW}		50			ns
Data-to-Segment Delay	t_{DSPD}				2.25	ms

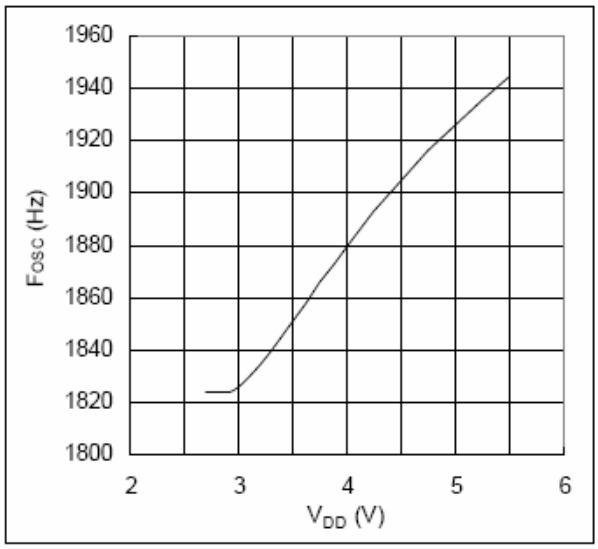
Typical Characteristics

(V_{DD}=5V, R_{EST}=9.53Ω, T_{AMB}=25℃ (unless otherwise specified).)

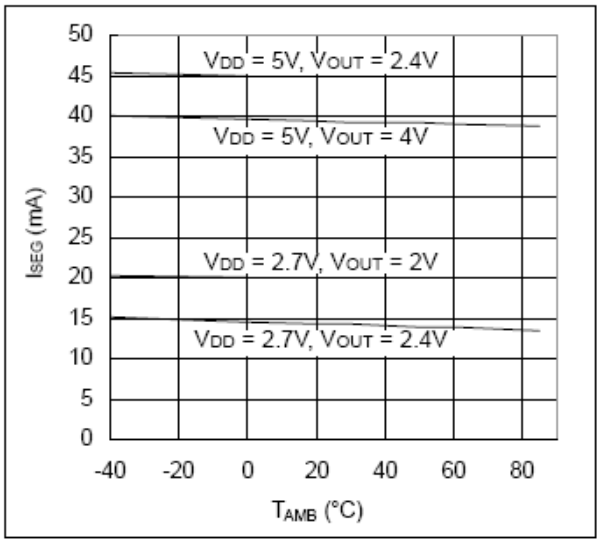
1.Scan Frequency vs. Temperature



2. Scan Frequency VS. V_{DD}



3. I_{SEG} VS. Temperature



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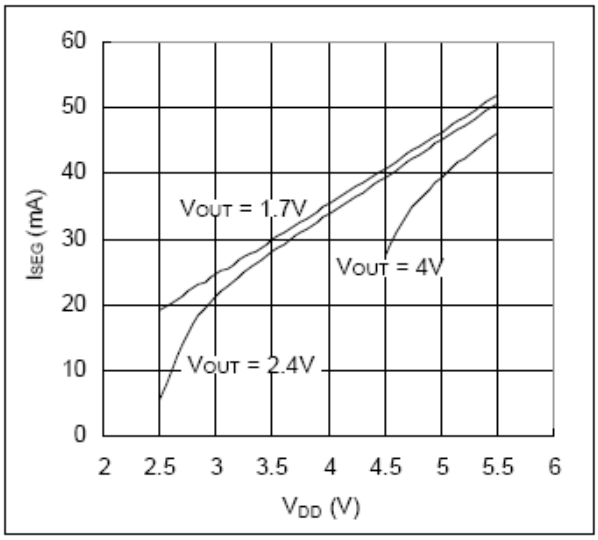
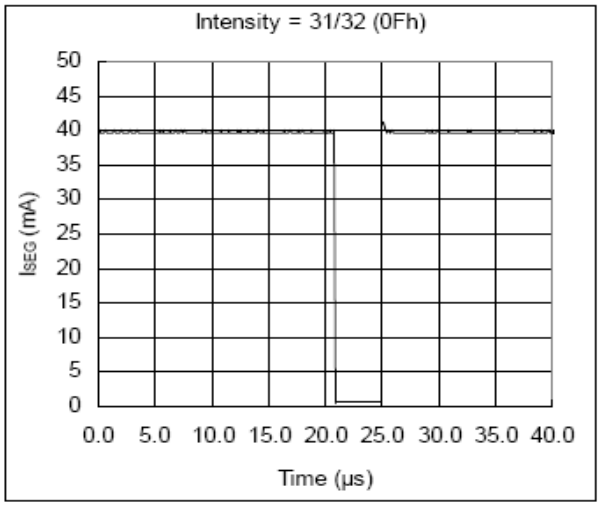
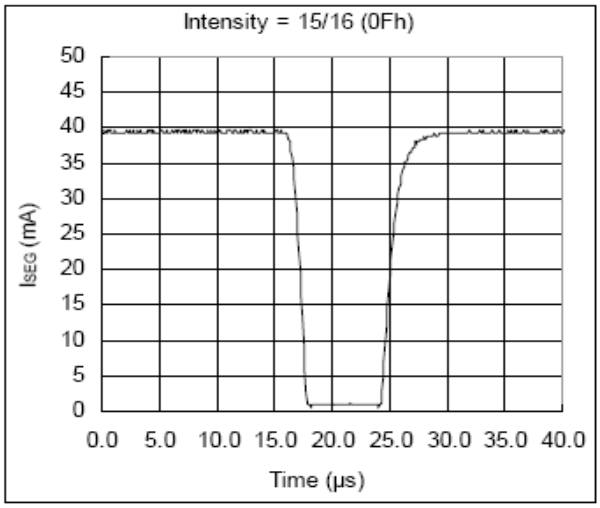


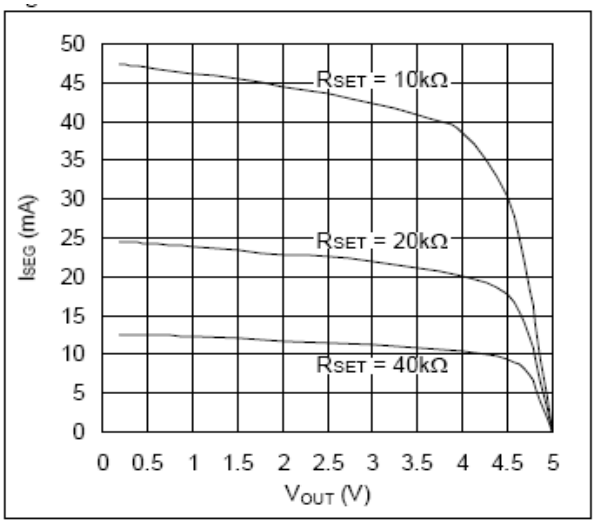
5. I_{SEG} VS. V_{OUT}



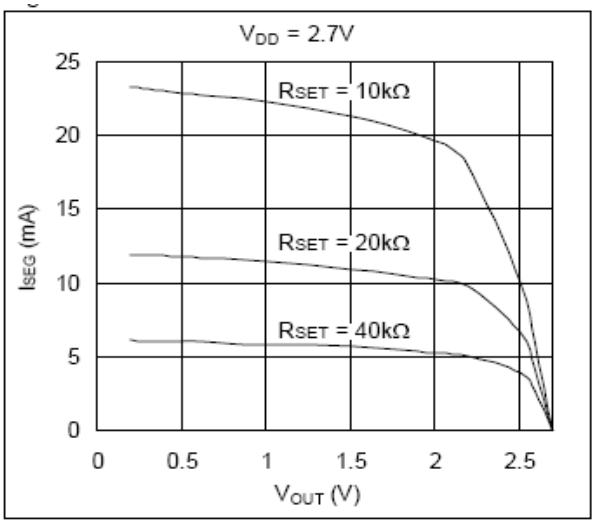
6. I_{SEG} VS. V_{OUT}



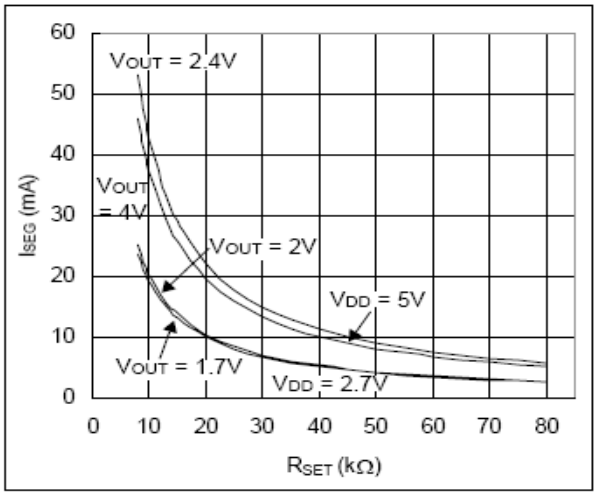
7. I_{SEG} vs. V_{OUT}



8. I_{SEG} vs. V_{OUT}



9. I_{SEG} vs. R_{SET}



Application Information

The A8478-A and A8478-B are identical except for three features:

- A8478-A segment driver is slew-rate limited to reduce electromagnetic interference (EMI).
- A8478-A serial interface is fully SPI compatible
- A8478-B is programmable.

Serial-Addressing Format

Programming the A8478 is done by writing to the device's internal registers (see Digit-and Control-Registers) via the 4-wire serial interface. A programming sequence consists of 16-bit packages as depicted in Table 1. The data is shifted into the internal 16-bit register with the rising edge of the CLK signal. With the rising edge of the LOAD/CSN signal the data is latched into a digit-or control-register. The LOAD/CSN signal must go high after the 16^{th} rising clock edge.

The LOAD/CSN signal can also come later but this must happen just before the next rising edge of CLK, otherwise the data will be lost. The contents of the internal shift register are applied 16.5 clock cycles later to pin D_{OUT}. The data is clocked out at the falling edge of CLK.

The first 4 bits (D15:D12) are "don't care" settings, bits D11:D8 contain the register address, and bits D7:D0 contain the data. The first bit is D15, the most significant bit (MSB). The exact timing is show in Fig. 1.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	Register Address (see table 2)				MSB			Data				LSB

Table 1: 16-Bit Serial Data Format

Initial Power-Up

On initial power-up, the A8478 register is reset to their default values, the display is blanked, and the A8478 goes into shutdown mode. All registers should be programmed for normal operation.

Note: the default settings enable only scanning of one digit; the internal decoder is disabled and the intensity control Register is set to the minimum values.

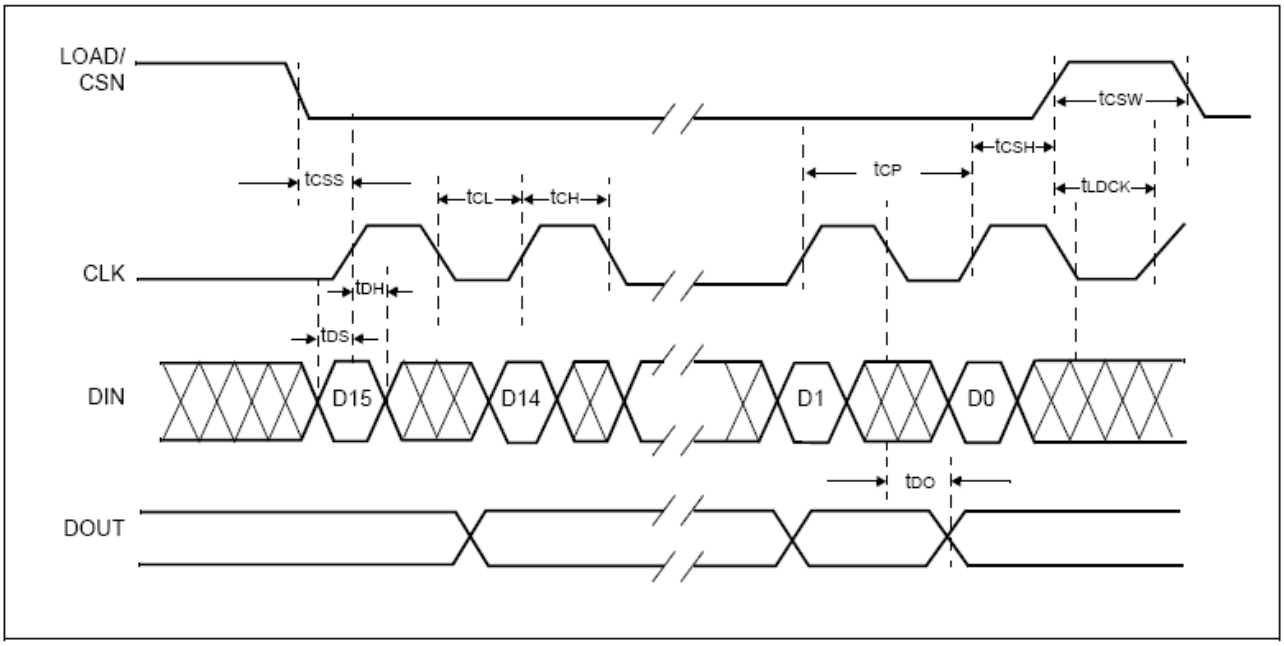


Fig. 1: Interface Timing

Shutdown Mode

The A8478 features a shutdown mode, consuming only 10uA (max) current. Shutdown mode is entered via a write the Shutdown Register (see Table 3). At that point, all segment current sources are pulled to ground and all digits drivers are connected to V_{DD}, so that all segments are blanked. The 8478-A behavior is identical except the drivers are high impedance.

Note: during shutdown mode the Digit-Registers maintain their data.

Shutdown mode can either be used as a means to reduce power consumption or for generating a flashing display (repeatedly entering and leaving shutdown mode). For minimum supply current in shutdown mode, logic input should be at GND or V_{DD} (CMOS logic level).

The A8478 need typically 250us to exit shutdown mode, and during shutdown mode the A8478 is fully programmable. Only the display test mode overrides shutdown mode.

When entering or leaving shutdown mode, the feature Register is reset to its default values (all 0s) when Shutdown Register bit D7 = 0.

Note: If the A8478 is used with an external clock, Shutdown Register bit D7 should be set to 1 when writing to the Shutdown Register.

Digit-and Control-Registers

The A8478 contains 8 Digit-Registers and 6 control-registers, which are listed in Table 2. All registers are selected using a 4-bit address word, and communication is done via the serial interface.

- Digit Registers – These registers are realized with an on-chip 64-bit memory. Each digit can be controlled directly without rewriting the whole register contents.
- Control Registers – These registers consist of decode mode, display intensity, number of scanned digits, shutdown, display test and features election registers.

Register	HEX Code	Address				
		D15:D12	D11	D10	D9	D8
No-Op	0xX0	X	0	0	0	0
Digit 0	0xX1	X	0	0	0	1
Digit 1	0xX2	X	0	0	1	0
Digit 2	0xX3	X	0	0	1	1
Digit 3	0xX4	X	0	1	0	0
Digit 4	0xX5	X	0	1	0	1
Digit 5	0xX6	X	0	1	1	0
Digit 6	0xX7	X	0	1	1	1
Digit 7	0xX8	X	1	0	0	0
Decode-Mode	0xX9	X	1	0	0	1
Intensity Control	0xXA	X	1	0	1	0
Scan Limit	0xXB	X	1	0	1	1
Shutdown	0xXC	X	1	1	0	0
N/A	0xXD	X	1	1	0	1
Feature	0xXE	X	1	1	1	0
Display Test	0xXF	X	1	1	1	1

Table 2: Register Address Map

Note: when Shutdown Register bit D7=1, the Feature Register is left unchanged when entering or leaving shutdown mode.

Shutdown Register (0xXC)

Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode Reset Feature Register to Default Settings	0x00	0	X	X	X	X	X	X	0
Shutdown Mode, Feature Register Unchanged	0x80	1	X	X	X	X	X	X	0
Normal Operation Reset Feature Register to Default Settings	0x01	0	X	X	X	X	X	X	1
Normal Operation, Feature Register Unchanged	0x81	1	X	X	X	X	X	X	1

Table 3: Shutdown Register Format 〔Address (HEX)=0xXC〕

Decode Enable Register (0xX9)

The Decode Enable Register sets the decode mode. BCE/HEX decoding (either BCD code – Characters 0:9, E, H, L, P, and -, or HEX code – characters 0:9 and A:F) is selected by bit D2 of the Feature Register. The Decode Enable Register is used to select the decode mode or no-decode for each digit. Each bit in the Decode Enable Register corresponds to its respective display digit (i.e., bit D0 corresponds to digit 0, bit D1 corresponds to digit 1 and so on). Table 5 lists some examples of the possible settings for the Decode Enable Register bits.

Note: A logic high enables decoding and a logic low bypasses the decoder altogether.

When decode mode is used, the decoder looks only at the lower-nibble (bits D3:D0) of the data in the Digit-Register, disregarding bits D6:D4. Bit D7 sets the decimal point (SEG DP) independent of the decoder and is positive logic (bit D7=1 turns the decimal point on). Table 5 lists the code-B font; Table 6 lists the HEX font. When no-decode mode is selected, data bits D7:D0 of the Digit-Registers correspond to the segment lines of the A8478. Table 7 shows the 1:1 pairing of each data bit and the appropriate segment line.

Decode Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
No decode for digits 7:0	0x00	0	0	0	0	0	0	0	0
Code-B/HEX decode for digit 0. No decode for digits 7:1	0x01	0	0	0	0	0	0	0	1
Code-B/HEX decode for digits 3:0. No decode for digits 7:4	0x0F	0	0	0	0	1	1	1	1
Code-B/HEX decode for digits 7:0	0xFF	1	1	1	1	1	1	1	1

Table 4: Decode Enable Register Format 〔address (HEX)=0xX9〕

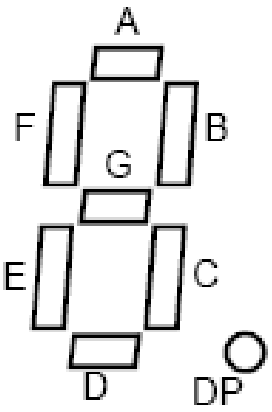


Fig 2: Standard 7-Segment LED

7-Segment Character	Register Data							On Segments=1						
	D7*	D6:D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	1	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
-		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
Blank		X	1	1	1	1		0	0	0	0	0	0	0

Table 5: Code-B Font (*The decimal point is enabled by setting bit D7=1)

7-Segment	Register Data							On Segments = 1						
Character	D7*	D6:D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
A		X	1	0	1	0		1	1	1	0	1	1	1
b		X	1	0	1	1		0	0	1	1	1	1	1
C		X	1	1	0	0		1	0	0	1	1	1	0
d		X	1	1	0	1		0	1	1	1	1	0	1
E		X	1	1	1	0		1	0	0	1	1	1	1
F		X	1	1	1	1		1	0	0	0	1	1	1

Table 6: HEX Font (*The decimal point is enabled by setting bit D7=1)

	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

Table 7: No-Decode Mode Data Bits and Corresponding Segment Lines

DISPLAY-Test Register (0xXF)

The A8478 can operate in two modes: normal mode and display test mode. In display test mode all LEDs are switched on at maximum brightness (duty cycle is 15/16 (A8478-B) or 31/32(A8478-A)). The A8478 remains in display-test mode until the Display-test Register is set for normal operation.

Note: all settings of the Digit-and Control-Registers are maintained.

Mode	Register Data							
	D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	X	X	X	X	X	X	X	0
Display Test Mode	X	X	X	X	X	X	X	1

Table 8: Display-Test Register Format 〔Address (HEX)=0xXF〕

Intensity Control Register (0xXA)

The brightness of the display can be controlled by digital means using the intensity control Register and by analog means using R_{SET} (see Selecting R_{SET} Resistor Value and Using External Drivers). Display brightness is controlled by an integrated pulse-width modulator which is controlled by the lower-nibble of the Intensity Control Register. The modulator scales the average segment-current in 16 steps from a maximum of 31/32 down to 1/32 (15/16 to 1/16 for the A8478-A) of the peak current set by $R_{SET.}$

Duty Cycle		HEX Code	Register Data							
A8478-A	A8478-B		D7	D6	D5	D4	D3	D2	D1	D0
1/16 (min on)	1/32 (min on)	0xX0	X	X	X	X	0	0	0	0
2/16	3/32	0xX1	X	X	X	X	0	0	0	1
3/16	5/32	0xX2	X	X	X	X	0	0	1	0
4/16	7/32	0xX3	X	X	X	X	0	0	1	1
5/16	9/32	0xX4	X	X	X	X	0	1	0	0
6/16	11/32	0xX5	X	X	X	X	0	1	0	1
7/16	13/32	0xX6	X	X	X	X	0	1	1	0
8/16	15/32	0xX7	X	X	X	X	0	1	1	1
9/16	17/32	0xX8	X	X	X	X	1	0	0	0
10/16	19/32	0xX9	X	X	X	X	1	0	0	1
11/16	21/32	0xXA	X	X	X	X	1	0	1	0
12/16	23/32	0xXB	X	X	X	X	1	0	1	1
13/16	25/32	0xXC	X	X	X	X	1	1	0	0
14/16	27/32	0xXD	X	X	X	X	1	1	0	1
15/16	29/32	0xXE	X	X	X	X	1	1	1	0
15/16(max on)	31/32 (max on)	0xXF	X	X	X	X	1	1	1	1

Table 9: Intensity Register Format (Address (HEX)=0xXA))

Scan-Limit Register (0x0B)

The Scan-Limit Register Controls which of the digits are to be displayed. When all 8 digits are to be displayed, the update frequency is typically $800H_{Z.}$ If the number of digits displayed is reduced, the update frequency is increased. The frequency can be calculated using 8fOCS/N, where N is the number of digits. Since the number of displayed digits influences the brightness, R_{SET} should be adjusted accordingly. Table 11 lists the maximum allowed current when fewer than 4 digits are used.

Note: To avoid differences in brightness this register should not be used to blank parts of the display (leading zeros).

Scan Limit	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Display digit 0 only (see Table 11)	0xX0	X	X	X	X	X	0	0	0
Display digits 0:1 (see Table 11)	0xX1	X	X	X	X	X	0	0	1
Display digits 0:2 (see Table 11)	0xX2	X	X	X	X	X	0	1	0
Display digits 0:3	0xX3	X	X	X	X	X	0	1	1
Display digits 0:4	0xX4	X	X	X	X	X	1	0	0
Display digits 0:5	0xX5	X	X	X	X	X	1	0	1
Display digits 0:6	0xX6	X	X	X	X	X	1	1	0
Display digits 0:7	0xX7	X	X	X	X	X	1	1	1

Table 10: Scan-Limit Register Format 〔Address(HEX)=0xXB)〕

Number of Digits Displayed	Maximum Segment Current (mA)
1	10
2	20
3	30

Table 11: Maximum Segment Current for 1-,2-,or 3-Digit Displays

Feature Register (0xXE)

The Feature Register is used for switching the device into external clock mode, applying an external reset, selecting code-B or HEX decoding, enabling or disabling blinking, enabling or disabling the SPI-compatible interface (A8478-B only), setting the blinking rate, and resetting the blink timing.

Note: At power-up the Feature Register is initialized to 0.

D7	D6	D5	D4	D3	D2	D1	D0
BLINK_START	SYNC	BLINK_FREQ_SEL	BLINK_EN	SPI_EN	DECODE_SEL	REQ_RES	CLK_EN

Table 12: Feature Register Summary

Addr:0xXE		Feature register		
		Enables and disables various device features		
Bit	**Bit Name**	**default**	**access**	**Bit Description**
D0	CLK_EN	0	R/W	External clock active 0=Internal oscillator is used for system clock 1=Pin CLK of the serial interface operates as system clock input
D1	REG_RES	0	R/W	Resets all control registers except the Feature Register 0=Reset disabled. Normal operation 1=All control registers are reset to default state (except the Feature Register) identically after power-up Note: The Digit Registers maintain their data
D2	DECODE_SEL	0	R/W	Selects display decoding 0=Enable Code-B decoding (see Table 5) 1=Enable HEX decoding (see Table 6)
D3	SPI_EN	0	R/W	Enables the SPI-compatible interface 0=Disable SPI-compatible interface(A8478-B only) 1=Enable the SPI-compatible interface(8478-B only) Note: The SPI-compatible interface is always enabled in the A8478-A
D4	BLINK_EN	0	R/W	Enables blinking 0=Disable blinking 1=Enable blinking
D5	BLINK_FREQ_SEL	0	R/W	Sets blink with low frequency (with the internal oscillator enabled) 0=Blink period typically is 1 second(0.5s on, 0.5s off) 1=blink period is 2 second (1s on, 1s off)
D6	SYNC	0	R/W	Synchronizes blinking on the rising edge of pin LOAD/CSN. The multiplex and blink timing counter is cleared on the rising edge of pin LOAD/CSN. By setting this bit in multiple A8478 devices, the blink timing can be synchronized across all the devices.
D7	BLINK_START	0	R/W	Start Blinking with display enabled phase. When bit D4 (blink_en) is set, bit D7 determines how blinking starts. 0=Blinking starts with the display turned off 1=Blinking starts with the display turned on

Table 13: Feature Register Bit Descriptions 〔Address (HEX)=0xXE)〕

No-OP Register (0xX0)

The no-Op Register is used when multiple A8478 advices are cascaded in order to support displays with more than 8 digits. The cascading must be done in such a way that all D_{OUT} pins are connected to D_{IN} of the next A8478 (see Fig. 3). The LOAD/CSN and CLK signals are connected to all devices.

For example, if five devices are cascaded, in order to perform a write operation to the fifth device, the write-command must be followed by four no-operation commands. When the LOAD/CSN signal goes high, all shift registers are latched. The first four devices will receive no-operation commands and only the fifth device will receive the intended operation command, and subsequently update its register.

Supply Bypassing and Wiring

In order to achieve optimal performance the A8478 should be placed very close to the LED display to minimize effects of electromagnetic interference and wiring inductance.

Furthermore, a 10uF electrolytic and a 0.1uF ceramic capacitor should be connected between pins V_{DD} and GND to avoid power supply ripple (see Fig. 3).

Note: Both GND pins must be connected to ground.

Selecting R_{SET} Resistor Value and Using External Drivers

Brightness of the display segments is controlled via R_{SET}. The current that flows between V_{DD} and I_{SET} defines the current that flows through the LEDS.

Segment current is about 200 times the current in I_{SET}. Typical values for R_{SET} for different segment currents, operating voltages, and LED voltage drop (V_{LED}) are given in Tables 14-18. The maximum current the A8478 can drive is 40mA. If higher currents are needed, external drivers must be used, in which case it is no longer necessary that the device drive high currents.

In cases where the device drives only a few digits, Table 11 specifies the maximum currents, and R_{SET} must be set accordingly.

Note: The display brightness can also be logically controlled (see Intensity Control Register (0xXA))

I_{SEG} (mA)	V_{LED} (V)	
	1.5	**2.0**
40	5kΩ	4.4kΩ
30	6.9kΩ	5.9kΩ
20	10.7kΩ	9.6kΩ
10	22.2 kΩ	20.7kΩ

Table 14: R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD}=2.7V

I_{SEG} (mA)	V_{LED} (V)		
	1.5	2.0	2.5
40	6.7kΩ	6.4kΩ	5.7kΩ
30	9.1kΩ	8.8kΩ	8.1kΩ
20	13.9kΩ	13.3kΩ	12.6kΩ
10	28.8kΩ	27.7kΩ	26kΩ

Table 15: R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD}=3.3V

I_{SEG} (mA)	V_{LED} (V)			
	1.5	2.0	2.5	3.0
40	7.5kΩ	7.2kΩ	6.6kΩ	5.5kΩ
30	10.18kΩ	9.8kΩ	9.2kΩ	7.5kΩ
20	15.6kΩ	15kΩ	14.3kΩ	13kΩ
10	31.9kΩ	31kΩ	29.5kΩ	27.3kΩ

Table 16: R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD}=3.6V

I_{SEG} (mA)	V_{LED} (V)				
	1.5	2.0	2.5	3.0	3.5
40	8.6kΩ	8.3kΩ	7.9kΩ	7.6kΩ	5.2kΩ
30	11.6kΩ	11.2kΩ	10.8kΩ	9.9kΩ	7.8kΩ
20	17.7kΩ	17.3kΩ	16.6kΩ	15.6kΩ	13.6kΩ
10	36.89kΩ	35.7kΩ	34.5kΩ	32.5kΩ	29.1kΩ

Table 17: R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD}=4.0

I_{SEG} (mA)	V_{LED} (V)					
	1.5	2.0	2.5	3.0	3.5	4.0
40	11.35kΩ	11.12kΩ	10.84kΩ	10.49kΩ	10.2kΩ	9.9kΩ
30	15.4kΩ	15.1kΩ	14.7kΩ	14.4kΩ	13.6kΩ	13.1kΩ
20	23.6kΩ	23.1kΩ	22.6kΩ	22kΩ	21.1kΩ	20.2kΩ
10	48.9kΩ	47.8kΩ	46.9kΩ	45.4kΩ	43.8kΩ	42kΩ

Table 18: R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD}=5.5V

Application Example

8X8 LED Dot Matrix Driver

The application example in Fig. 3 shows the A8478-B as a 8x8 LED Dot Matrix Driver.

The LED columns have common cathodes and are connected to the DIG0:7 outputs. The rows are connected to the segment drivers. Each of the 64 LEDs can be addressed separately. The columns are selected via the digits as listed in Table 2.

The Decode Enable Register must be set to '00000000' as described in Table 4. Single LEDs in a column can be addressed as described in Table 7. where bit D0 corresponds to segment G and bit D7 corresponds to segment DP.

Note: For a multiple-digit dot matrix, multiple A8478-B devices must be cascaded.

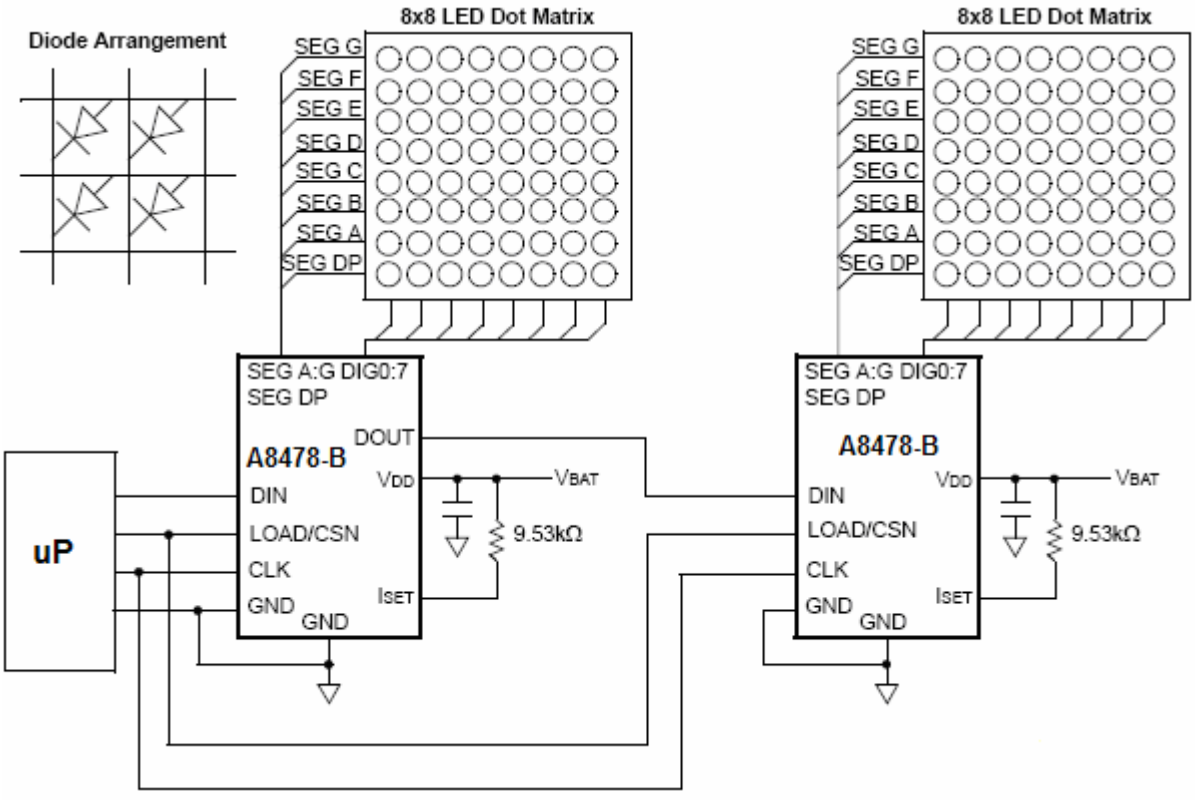


Fig. 3: Application Example as LED Dot Matrix Driver

Cascading Drivers

The example drives 2 dot matrix digits using a 4-wire microprocessor interface. All Scan-Limit Registers should be set to the same value so that not appear brighter than the other.

For example, to display 12 digits, set both Scan-Limit Registers to display 6 digits so that both displays have a 1/6 duty cycle per digit. If 11 digits are needed, set both Scan-Limit Registers to display 6 digits and leave one digit unconnected. Otherwise, if one driver is set to display 6 digits and the other to display 5 digits one display will appear brighter because its duty cycle per digit will be 1/5 and the other display's duty cycle will be 1/6.

Note: Refer to No-Op Register (0xX0) for additional information;

Calculating Power Dissipation

The upper limit for power dissipation (P_D) for the 8478 is determined from the following equation:

$$P_D = (V_{DD} \times 1mA) + (V_{DD} - V_{LED})(DUTY \times I_{SEG} \times N)$$

Where:

V_{DD} is the supply voltage

DUTY is the duty cycle set by intensity register

N is the number of segments driver (worst case is 8)

V_{LED} is the LED forward voltage

I_{SEG} = segment current set by R_{SET}

Dissipation Example:

I_{SEG} = 40mA, N = 8, DUTY = 31/32, V_{LED} = 1.8V at 40mA, $_{VDD}$ = 5.25V

P_D = 5.25V(1mA) + (5.25 V – 1.8V)(31/32 x 40mA x 8) = 1.075W

Thus, for a DIP package θ_{JA} = +75℃/W (from Table 19), the maximum allowed T_{AMB} is given by:

$T_{J,MAX} = T_{AMB} = P_D \times \theta_{JA}$ = 150℃ = T_{AMB} + 1.07W x 75℃/W

Where:

T_{AMB} = +69.4℃

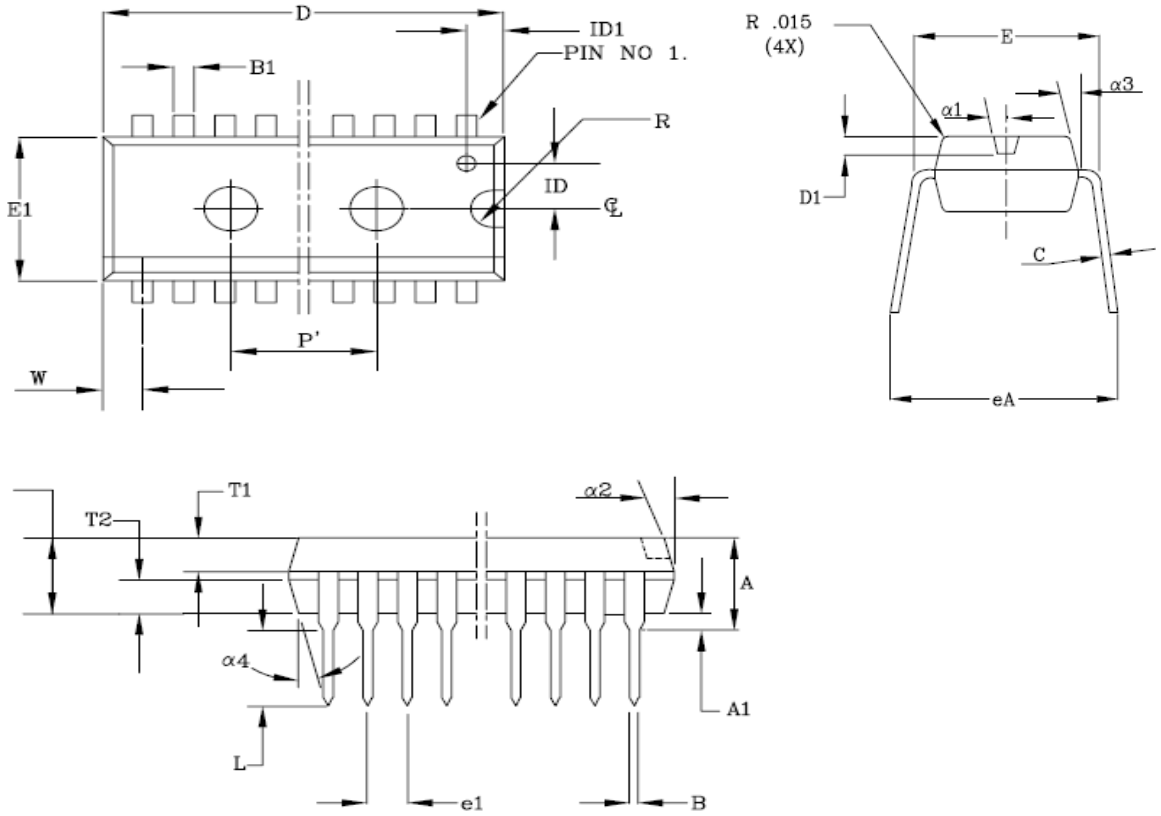
The T_{AMB} limit for SO Packages in the dissipation example above is +58.6℃

Package	Thermal Resistance (θ_{JA})
24 Narrow DIP	+75℃/W
24 SOP	+85℃/W

Table 19: Package Thermal Data

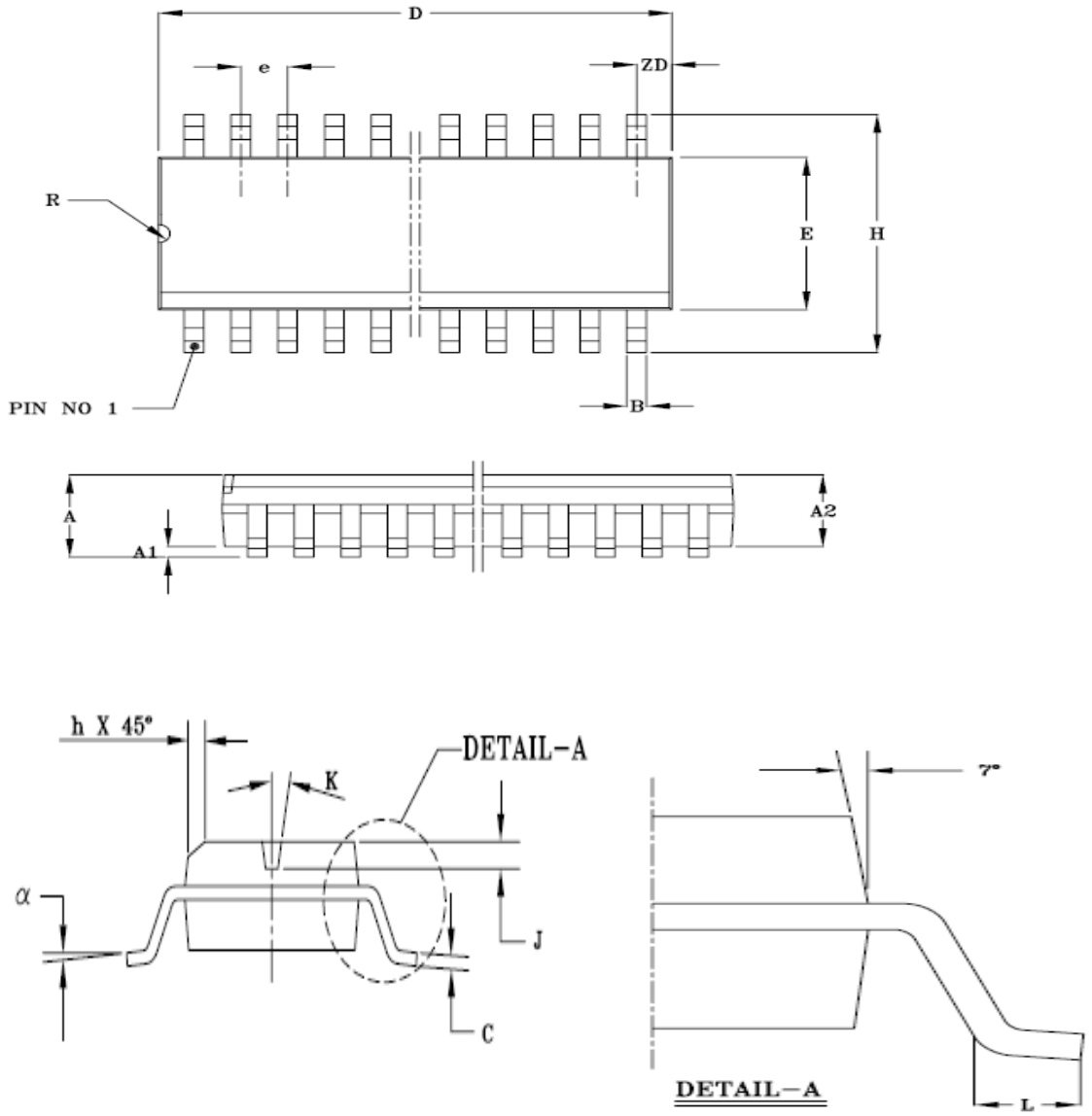
Packaging Information

Dimension in 24-pin Narrow DIP Package (Unit: mm)



Symbol	Min	Max
B	0.18	
B1	0.15	
C	0.10	
D	1.16	
D1	0.3	
E	0.295	
ID	0.64	
ID1	0.64	
E1	0.26	
eA	0.32	0.37
e1	1.00	
L	0.125	
R	0.03	
T	0.13	
T1	0.06	
T2	0.06	
W	0.03 REF	
α	7°	
α2	7°	
α3	7°	
α4	7°	
P	0.76	
A	0.145	0.17
A1	0.015	0.04

Dimension in 24-pin SOP Package (Unit: mm)



Symbol	Min	Max	Symbol	Min	Max
A	2.44	2.84	H	10.11	10.51
A1	0.10	0.30	h	0.31	0.71
A2	2.24	2.44	J	0.53	0.73
B	0.36	0.46	K	7° BSC	
C	0.23	0.32	L	0.51	1.01
D	12.65	12.85	R	0.63	0.89
E	7.40	7.5	ZD	0.66REF	
e	1.27 BSC		α	0°	8°

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