7 SEGMENT NUMERIC DISPLAYS
10MHz SERIAL INTERFACE, UP TO 8-DIGIT LED DRIVER

A8468

Description

The A8468 is an LED driver for 7 segment numeric displays of up to 8 digits. The A8468 can be programmed via a convention 4 wire serial interface. A8468 includes a BCD code-B decoder, a multiplex scan circuitry, segment and display drivers and a 64 Bit memory which is used to store the LED settings that continuo us reprogramming is unnecessary.

A8468 each individual segment can be addressed and updated separately. Only one external resistor to set the current through the LED display. Brightness can be controlled either in an analog or digital way and A8468 can choose the internal cod e-B decoder to display numeric digits or to address each segment directly.

The A8468 also includes low-power shutdown current at 20uA and an extremely low operating current 0.5mA in open loop and the number of visible digits can be programmed as well.

The A8468 can be reset by software and an external clock and several test modes support for debugging easier.

The A8468 is available in 24pin DIP and SOP package.

Ordering Information

24pin Narrow DIP	A8468PN24 (Tube)
24pin SOP	A8468M24 (Tube) A8468M24R (T/R)

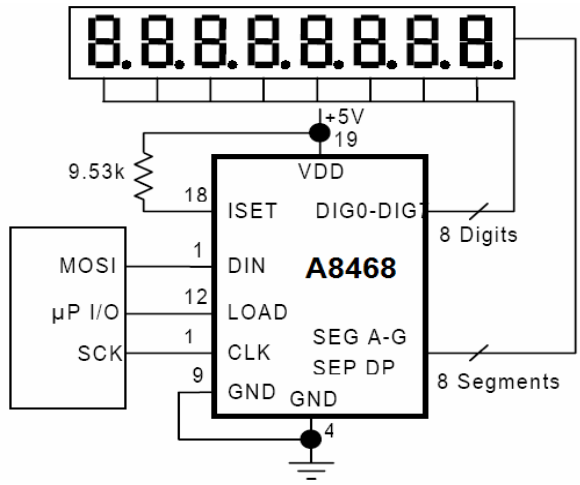
Features

- 20uA Low-Power Shutdown (Data Retained)
- Extremely Low Operating Current 0.5mA in Open Loop
- 10MHz Serial Interface
- Optional External Clock
- Individual LED Segment Control
- Decode/No-Decode Digit Selection
- Digital and Analog Brightness Control
- Drive Common-Cathode LED Display
- Software Reset
- 24pin DIP and SOP Package

Application

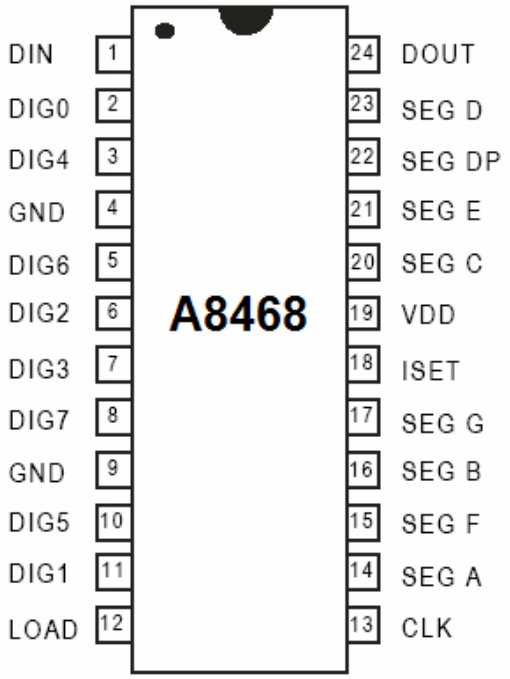
- LED Matrix Displays
- White Goods
- Panel Meters
- Bar-Graph Displays
- Industrial Controllers

Typical Application



8-Digit uP Display

Pin Description



Pin #	Name	Function
1	DIN	Data input. Data is programmed into the 16Bit shift register on the rising CLK edge.
2,3	DIG0, DIG4	2 of 8 digit driver lines that sink the current from the common cathode of the display in shutdown mode the A8468 switches the outputs to VDD.
4	GND	Ground pin, must be connected.
5-8	DIG6,2,3,7	4 of 8 digit driver lines that sink the current from the common cathode of the display in shutdown mode the A8468 switches the outputs to VDD.
9	GND	Ground pin, must be connected.
10,11	DIG5, DIG1	2 of 8 digit driver lines that sink the current from the common cathode of the display in shutdown mode the A8468 switches the outputs to VDD.
12	LOAD	Strobe input. With the rising edge of the LOAD signal the 16Bit of serial data is latched into the register.
13	CLK	Clock Input. The interface is capable to support clock frequency up to 10MHz. The serial data is clocked into the internal shift register with the rising edge of the CLK signal. On the DOUT pin the data is applied with the falling edge of CLK.
14-17	SEGA,F,B,G	4 of 7 segment driver lines including the decimal point. When a segment is turned off the output is connected to GND.
18	ISET	The current into ISET determines the peak current through the segments and therefore the brightness.
19	VDD	Positive Supply Voltage (+5V)
20-23	SEGC,E,DP,D	3 of 7 segment driver lines including the decimal point. When a segment is turned off the output is connected to GND.
24	DOUT	Serial data output for cascading drivers. The output is valid after 16.5 clock cycles. The output is never set to high impedance.

Absolute Maximum Ratings

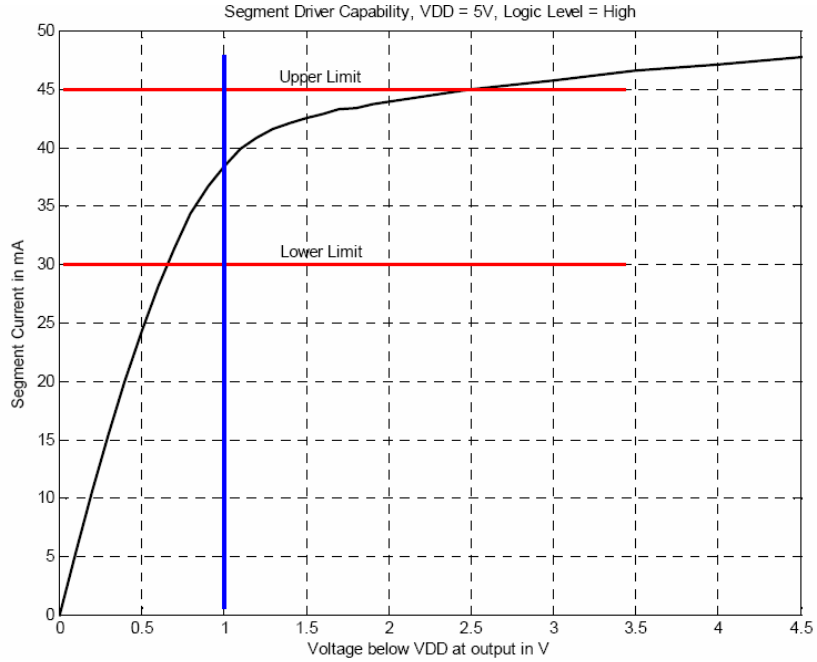
Voltage (with respect to GND)	
V_{DD}	-0.3~6V
DIN, CLK, LOAD	-0.3~6V
All Other Pins	-0.3~(V_{DD}+0.3V)
Current	500mA
DIG0=-DIG7 Sink Current	100mA
SEGA-G, DP Source Current	260°C, 10S
Continuous Power Dissipation (T_A=+85°C)	
Narrow DIP (derate 13.3mW/°C above +70°C)	1066mW
SOP (derate 11.8mW/°C above +70°C)	941mW
Operating Temperature Range (T_{MIN} to T_{MAX})	-40°C ~ +85°C
Storage Temperature Range	-65°C ~ +150°C
Package Body Temperature	+240°C

Electrical Characteristics (V_{DD}=5V, R_{SET}=0.53kΩ±1%, T_A=T_{MIN} to T_{MAX}, unless otherwise noted.)

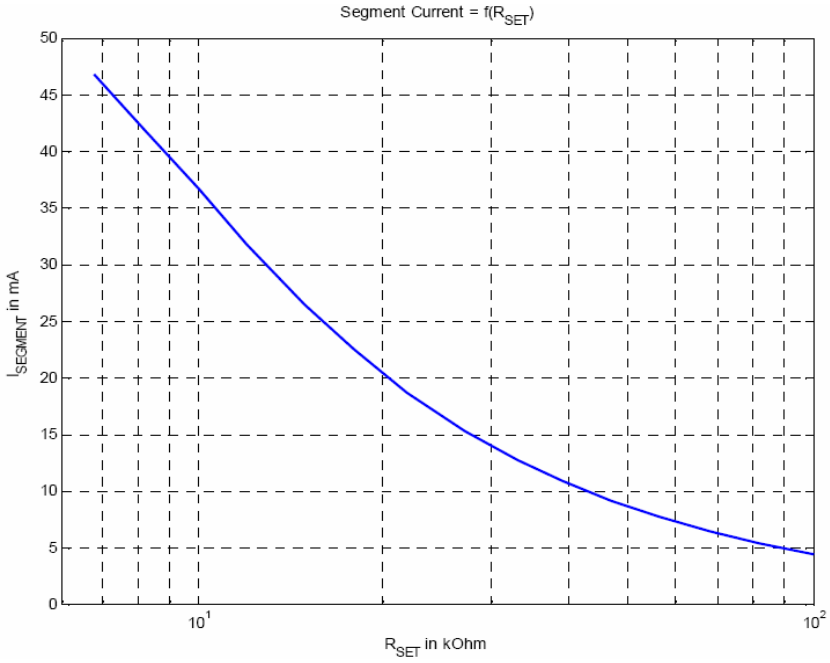
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Current DIN, CLK, LOAD	I_{IH}, I_{IL}	$V_{IN=0V}$ or V_{DD}	-1		1	uA
Logic High Input Voltage	V_{IH}		3.5			V
Logic Low Input Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	D_{OUT}, I_{SOURCE}=-1mA	V_{DD}-1			V
Output Low Voltage	V_{OL}	D_{OUT}, I_{Sink}= 1.6mA			0.4	V
Hysteresis Voltage	D_{VI}	DIN, CLK, LOAD		1		V
Timing Characteristics						
CLK Clock Period	t_{CP}		100			ns
CLK Pulse Width High	t_{CH}		50			ns
CLK Pulse Width Low	t_{CL}		50			ns
CLK Rise to LOAD Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		25			ns
DIN Hold Time	t_{DH}		0			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD}=50pF			25	ns
LOAD Rising Edge to Next Clock Rising Edge	t_{LDCK}		50			ns
Minimum Load Pulse High	t_{CSW}		50			ns
Data-to-Segment Delay	t_{DSPD}				2.25	ms

Typical Characteristics

1. Segment Driver Capability



2. Segment Current vs R_{SET}



Application Information

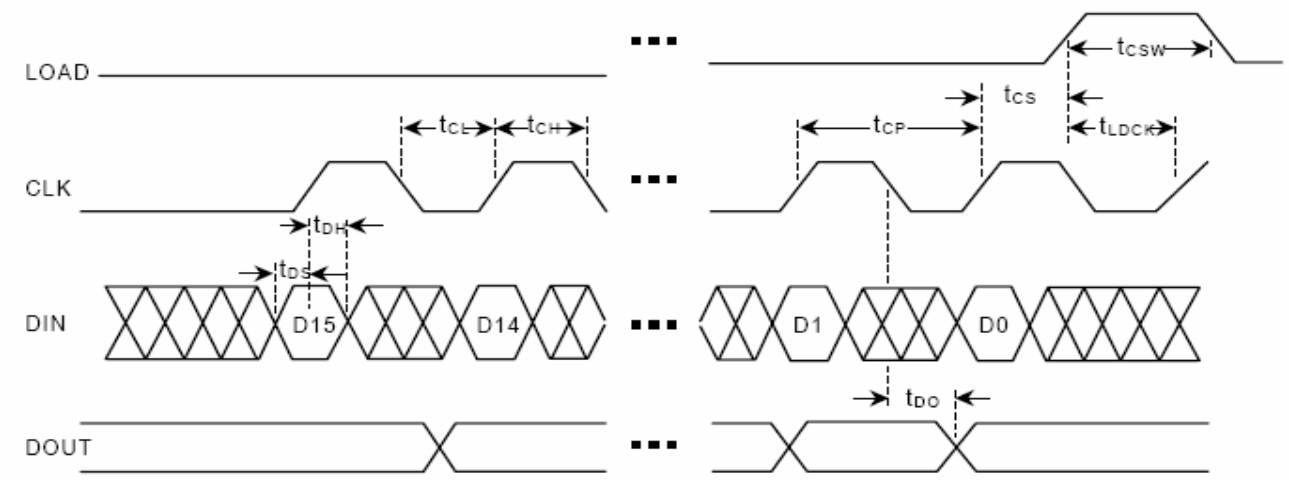


Fig 1: Timing Diagram

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	Address				MSB			Data				LSB

Table 1: Serial Data Format (16Bits)

Serial-Addressing Modes

Programming of the A8468 is done via the 4 wire serial interface. A programming sequence consists of 16-bit packages. The data is shifted into the internal 16Bit register with the rising edge of the CLK signal. With the rising edge of the LOAD signal the data is latched into a digital or control register depending on the address. The LOAD signal must go to high after the 16th rising clock edge. The LOAD signal can also come later but just before the next rising edge of CLK, otherwise data would be lost. The content of the internal shift register is applied 16.5 clock cycles later to the DOUT pin. The data is clocked out at the falling edge of CLK. The Bits of the 16Bit-programming package are described in Table 1. The first 4 Bits D15-12 don't care, D11-D8 contain the address and D7-D0 contain the data. The first bit is D15, the most significant bit (MSB). The exact timing is given in Fig 1.

Digit and Control Registers

The A8468 incorporates 15 registers, which are listed in Table 2. The digit and control registers are selected via the 4Bit address word. The 8 digit register are realized with a 16bit memory. Each digit can be controlled directly without rewriting the whole contents. The control registers consist of decode mode, display intensity, number of scanned digits, shutdown, display test and reset/external clock register.

Register	Address					Hex
	D15-D12	D11	D10	D9	D8	Code
No-OP	X	0	0	0	0	0xX0
Digit 0	X	0	0	0	1	0xX1
Digit 1	X	0	0	1	0	0xX2
Digit 2	X	0	0	1	1	0xX3
Digit 3	X	0	1	0	0	0xX4
Digit 4	X	0	1	0	1	0xX5
Digit 5	X	0	1	1	0	0xX6
Digit 6	X	1	1	1	1	0xX7
Digit 7	X	1	0	0	0	0xX8
Decode Mode	X	1	0	0	1	0xX9
Intensity	X	1	0	1	0	0xXA
Scan Limit	X	1	0	1	1	0xXB
Shutdown	X	1	1	0	0	0xXC
Not Used	X	1	1	0	1	0xXD
Reset and Ext. Clock	X	1	1	1	0	0xXE
Display Test	X	1	1	1	1	0xXF

Table 2: Register Address Map

Shutdown Mode

The A8468 includes a shutdown mode, where it consumes only 20uA current. The shutdown mode is entered via a write to register 9Ch. Then all segment current sources are pulled to ground and all digit drivers are connected to V_{DD}, so that nothing is displayed. All internal digit registers keep the programmed values. The shutdown mode can either be used for power saving or for generating a flashing display by repeatedly entering and leaving the shutdown mode. The A8468 needs typically 250us to exit the shutdown mode. During shutdown the A8468 is fully programmable. Only the display test function overrides the shutdown mode.

Initial Power-UP

After powering up the system all register are reset, so that the display is blank. The A8468 starts the shutdown mode. All registers should be programmed for normal operation. The default settings enable only scan of one digit, the internal decoder is disable, data register and intensity register are set to the minimum value.

Decode-Mode Register

A8468 includes a BCD code-B decoder. Every digit can be selected via register 0.9h to be decoded. The BCD code consists of the numbers 0=-9, E, H, L, P and -. In register 09h a logic high enables the decoder for the appropriate digit. In case that the decoder is bypassed (logic low) the data Bits D7-D0 correspond to the segment lines of the A8468. In Table 4 some possible settings for register 09h are shown. Bit D7, which corresponds to the decimal point, is not affected by the settings of the decoder. Logic high means that the decimal point is displayed. In Table 5 the font of the Code B decoder is shown. In Table 6 the correspondence of the register to the appropriate segments of a 7 segment display is shown (see Fig 2).

Mode	Address Code (Hex)	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode	0xXC	X	X	X	X	X	X	X	0
Normal Operation	0xXC	X	X	X	X	X	X	X	1

Table 3: Shutdown Register Format 〔Address (Hex)= 0xXC〕

Decode Mode	Register Data								Hex Code
	D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digits 7-0	0	0	0	0	0	0	0	0	0x00
Code B decode for digit 0 no decode for digits 7-1	0	0	0	0	0	0	0	1	0x01
Code B decode for digits 3-0 No decode for digits 7-4	0	0	0	0	1	1	1	1	0x0F
Code B decode for digits 7-0	1	1	1	1	1	1	1	1	0xFF

Table 4: Decode-mode Register Examples 〔Address (Hex)= 0xX9〕

7-Segment Character	Register Data							On Segments = 1						
	D7*	D6-D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		0	1	1	1	0	0	1
4		X	0	1	0	0		1	1	1	0	0	1	1
5		X	0	1	0	1		0	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		0	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		0	1	1	1	0	1	1
-		X	1	0	1	0		1	0	0	0	0	0	1
E		X	1	0	1	1		0	0	0	1	1	1	1
H		X	1	1	0	0		1	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
Blank		X	1	1	1	1		0	0	0	0	0	0	0

Table 5: Code B font (* The decimal point is set by bit D7=1)

	Register Data							
Corresponding	D7	D6	D5	D4	D3	D2	D1	D0
Segment Lin	DP	A	B	C	D	E	F	G

Table 6: No=-decode mode data bits and corresponding segment lines

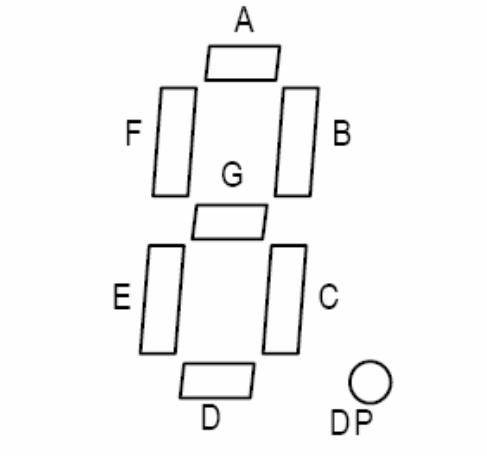


Fig 2: Standard 7-Setment LED

Intensity Control and Interdigit Blanking

Brightness of the display can be controlled in an analog way by changing the external resistor (R_{SET}). The current, which flows between V_{DD} and I_{SET}, defines the current that flows throught LEDs. The LED current is 100 times the I_{SET} current. The minimum value of R_{SET} should be 9.53kΩ , which corresponds to 40mA segment current. The brightness of the display can also be controlled digitally via register 0Ah. The brightness can be programmed in 16 sets and is shown in Table 7. An internal Pulse width Modulator controls the intensity of the display.

Scan-Limit Register

The scan limit register 8Bh selects the number of digits displayed. When all 8 digits are displayed the update frequency is typically 800Hz. If the number of digits displayed is reduced, the update frequency is reduced as well. The frequency can be calculated using 8fOSC/N, where N is the number of digits. Since the number of displayed digits influences the brightness, the resistor R_{SET} should be adjusted accordingly. Table 9 shows the maximum allowed current when fewer than 4 digits are used. To avoid differences in brightness the scan limit register should not be used to bank portions of the display (leading Zeros).

Duty Cycle	D7	D6	D5	D4	D3	D2	D1	D0	Hex Code
1/32 (min on)	X	X	X	X	0	0	0	0	0xX0
3/32	X	X	X	X	0	0	0	1	0xX1
5/32	X	X	X	X	0	0	1	0	0xX2
7/32	X	X	X	X	0	0	1	1	0xX3
0	X	X	X	X	0	1	0	0	0xX4
0	X	X	X	X	0	1	0	1	0xX5
1	X	X	X	X	0	1	1	0	0xX6
1	X	X	X	X	0	1	1	1	0xX7
0	X	X	X	X	1	0	0	0	0xX8
0	X	X	X	X	1	0	0	1	0xX9
1	X	X	X	X	1	0	1	0	0xXA
1	X	X	X	X	1	0	1	1	0xXB
0	X	X	X	X	1	1	0	0	0xXC
0	X	X	X	X	1	1	0	1	0xXD
1	X	X	X	X	1	1	1	0	0xXE
1	X	X	X	X	1	1	1	1	0xXF

Table 7: Intensity Register Format 〔Address (Hex)= 0xXA〕

Scan Limit	Register Data								Hex Code
	D7	D6	D5	D4	D3	D2	D1	D0	
Display digit 0 only	X	X	X	X	X	0	0	0	0xX0
Display digits 0 & 1	X	X	X	X	X	0	0	1	0xX1
Display digits 0 1 2	X	X	X	X	X	0	1	0	0xX2
Display digits 0 1 2 3	X	X	X	X	X	0	1	1	0xX3
Display digits 0 1 2 3 4	X	X	X	X	X	1	0	0	0xX4
Display digits 0 1 2 3 4 5	X	X	X	X	X	1	0	1	0xX5
Display digits 0 1 2 3 4 5 6	X	X	X	X	X	1	1	0	0xX6
Display digits 0 1 2 3 4 5 6 7	X	X	X	X	X	1	1	1	0xX7

Table 8: Scan-Limit Register Format 〔Address (Hex)= 0xXB〕

Number of Digits Displayed	Maximum Segment Current (mA)
1	10
2	20
3	30

Table 9: Maximum Segment Current for 1-, 2-, or 3-digit Displays

Display Test Register

With the display test register 0Fh all LED can be tested. In the test mode all LEDs are switched on at maximum brightness (duty cycle 31/32). All programming of digit and control registers is maintained. The format of the register is given in Table 10.

Mode	Register Data							
	D7	D6	D5	D4	D3	D2	D1	D0
Display digit 0 only	X	X	X	X	X	X	X	0
Display digits 0 & 1	X	X	X	X	X	X	X	1

Table 10: Display-Test Register Format 〔Address (Hex)= 0xXF〕

Note: The A8468 remains in display-test mode until the display-test register is reconfigured for normal operation.

No-Op Register (Cascading of A8468)

The no-operation register 00h is used when A8468 are cascaded in order to support more than 8 digit display. The cascading must be done in a way that all DOUT are connected to DIN of the following A8468. The LOAD and CLK signals are connected to all devices. For a write operation for example to the fifth device the command must be followed by four no-operation commands. When the LOAD signal finally goes to high all shift registers are latched. The first four devices have got no-operation commands and only the fifth device sees the intended command and updates its register.

Reset and External Clock Register

This register is addressed via the serial interfaced. It allows to switch the device to external clock mode (if D0=1 the CLK pin of the serial interface operates as system clock input) and to apply an external reset (D1). This bring all registers (except reg. E) to default state. For standard operation the register contents should be “00h”.

Mode	Address Code (Hex)	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation, Internal Clock	0xXE	X	X	X	X	X	X	0	0
Normal Operation, External Clock	0xXE	X	X	X	X	X	X	0	1
Reset State, Internal Clock	0xXE	X	X	X	X	X	X	1	0
Reset State, External Clock	0xXE	X	X	X	X	X	X	1	1

Table 11: Reset and External Clock Register 〔Address (Hex)= 0xXE〕

Supply Bypassing and Wiring

In order to achieve optimal performance the A8468 shall be placed very close to the LED display to minimize effects of electromagnetic interference and wiring inductance. Furthermore it is recommended to connect a 10uF electrolytic and a 0.1uF ceramic capacitor between V_{DD} and GND to avoid power supply ripple. Also, both GNDs must be connected to ground.

Selecting R_{SET} resistor and Using External Drivers

The current through the segments is controlled via the external resistor R_{SET} Segment current is about 100 times the current in I_{SET}. The right values for I_{SET} are given in Table 12. The maximum current the A8468 can drive is 40mA. If higher currents are needed, external drivers much be used. In that case it is no longer necessary that the A8468 drives high currents. A recommended value for R_{SET} is 47KΩ. In cases that the A8468 only drives few digits Table 9 specifies the maximum currents and R_{SET} must be set accordingly. Refer to absolute maximum ratings to calculate acceptable limits for ambient temperature, segment current, and the LED forward-voltage drop.

ISEG	VLED (V)				
(mA)	**1.5**	**2.0**	**2.5**	**3.0**	**3.5**
40	12.2	11.8	11.0	10.6	9.69
30	17.8	17.1	15.8	15.0	14.0
20	29.8	28.0	25.9	24.5	22.6
10	66.7	63.7	59.3	55.4	51.2

Table 12: R_{SET} vs. Segment Current and LED Forward Voltage

Application Example

8x8 LED Dot Matrix Driver

The example in Fig 3 uses the A8468 to drive and 8x8 LED Dot Matrix. The LED columns have common cathode and are connected to the DIG0-7 outputs. The rows are connected to the segment drivers. Each of the 64 LEDs can be addressed separately. The columns are selected via the digits as shown in Table 2. The decode mode register (9xX9) has to be programmed to “00000000” as stated in Table 4. The single LEDs in a column can be addressed as stated in Table6, where D0 corresponds to segment G and d/ to segment D0. For a multiple digit Dot Matrix several A8468 have to be cascaded.

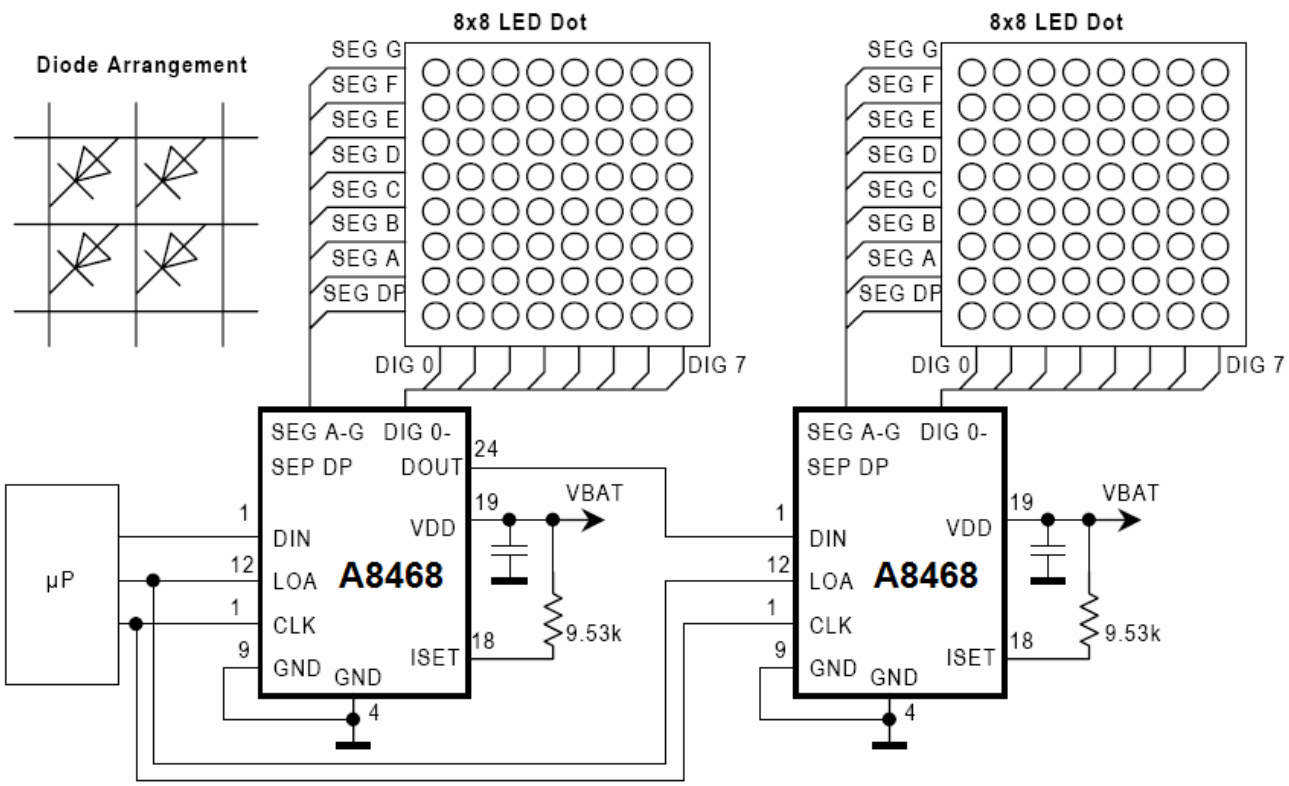


Fig 3: Application Example as LED Dot Matrix Driver

Cascading Drivers

The A8468 can be cascaded as well. Th DOUT pin must be connected to the DIN pin of the following A8468.

Computing Power Dissipation

The upper limit for dissipation (PD) for the A8468 is determined from the following equation:

$PD = (V_{DD} \times 0.5mA) + (V_{DD} – VL_{ED}) (DUTY \times I_{SEG} \times N)$

Where:

VDD=Supply Voltage

DUTY= Duty cycle set by intensity register

N=number of segments driven (worst case is 8)

V_{LED}=LED forward voltage

I_{SEG}=Segment current set by R_{SET}

Dissipation Example:

I_{SEG}=40mA, N=8, DUTY=31/32, V_{LED}=1.8V at 40mA, V_{DD}=5.25V

PD= 5.25V (0.5mA) + (5.25V- 1.8V) (31/32 x 40mA x 8) = 1.07W

Thus, for a DIP package θ_{JA}=+75°C/W (from Table 13), the maximum allowed ambient temperature T_A is given by: $T_{J,MAX} = T_A + PD \times \theta_{JA} = 150\,^{o}C = T_A + 1.07W \times 75^{o}C/W$

Where T_A = +69.7°C

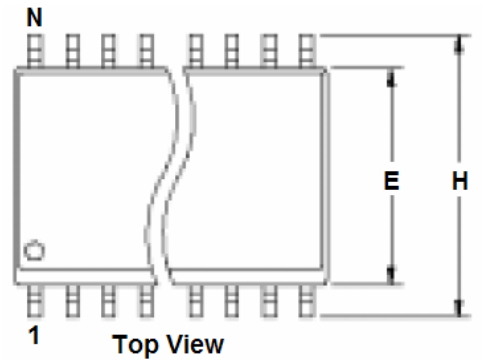
The T_A limit for SOP package in the dissipation example above is +59.0°C

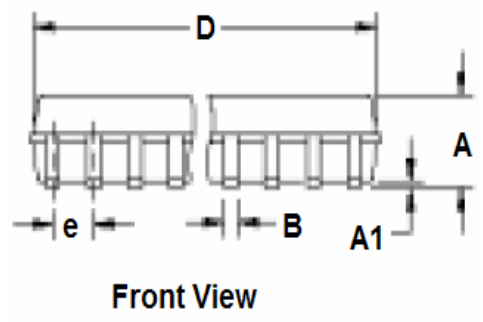
Package	Thermal Resistance (θ_{JA})
24-pin Narrow DIP	+75°C/W
24-pin SOP	+85°C/W
Maximum Junction Temperature (T_J)	+150°C
Maximum Ambient Temperature (T_A)	+85°C

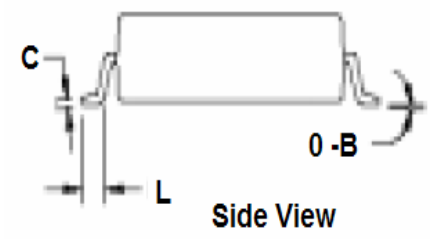
Table 13: Package Thermal Resistance Data

Package Information

Dimension in 24-pin SOP Package (Unit: mm)

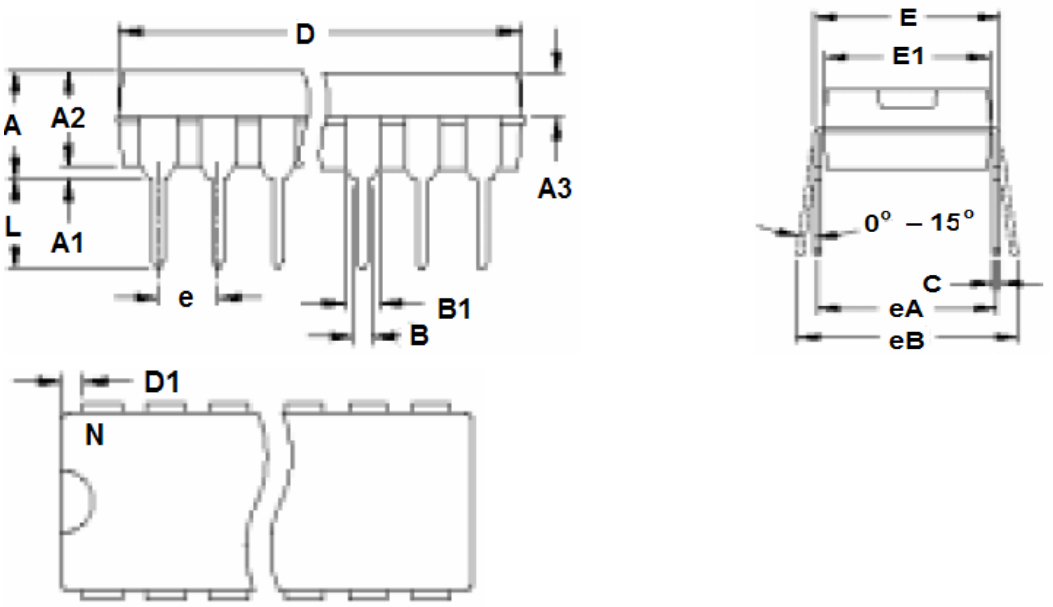






Inches			Millimeters	
Dim	**Min**	**Max**	**Min**	**Max**
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.2	15.6
e	0.050		1.27	
E	0.29	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

Dimension in 24-pin Narrow DIP Package (Unit: mm)



Inches			Millimeters	
Dim	**Min**	**Dim**	**Min**	**Dim**
A	---	0.180	---	4.572
A1	0.015	---	0.380	---
A2	0.125	0.0175	3.180	4.45
A3	0.055	0.080	1.400	2.030
B	0.015	0.022	0.381	0.560
B1	0.045	0.065	1.14	1.650
C	0.008	0.014	0.200	0.355
D	1.14	1.265	28.96	32.13
D1	0.005	0.080	0.130	2.030
E	0.300	0.325	7.62	8.260
E1	0.240	0.310	6.100	7.870
e	0.100 BSC		2.54 BSC	
eA	0.300 BSC		7.62 BSC	
eB	0.400 BSC		10.2 BSC	
L	0.115	0.150	2.921	3.810

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